Claims

We Claim,

1. A method of transmitting data in a transceiver system, comprising:

receiving K parallel data bits into a transmitter minimum data frequency multiplexer, where K is an integer;

determining whether a flip condition exists;

if the flip condition exists, flipping a selected subset of the K parallel data bits;

serializing the K parallel data bits to form a serialized bit stream; and

forming a clock signal with a signal indicating whether the flip condition exists or not.

2. The method of Claim 1, wherein determining whether a flip condition exists includes determining if all of the K parallel data bits are the same logic level.

3. The method of Claim 2, wherein determining whether a flip condition exists further includes determining whether an enable flag is set.

4. The method of Claim 1, wherein the selected subset of the K bits includes K/2 bits of the K bits.

5. The method of Claim 1, wherein forming a clock signal includes changing the duty cycle of the clock signal if the flip condition exists.

6. The method of Claim 5, wherein the duty cycle is reduced if the flip condition exists.

7. A method of receiving data, comprising:

receiving serialized data;

receiving a clock signal;

retrieving a flip signal from the clock signal;

flipping a subset of data bits in the serialized data if the flip signal indicates a flipped condition; and

deserializing the serialized data to form parallel data.

8. The method of Claim 7, wherein retrieving the flip signal from the clock signal includes

measuring the duty cycle of the clock signal; and

setting the flip signal if the duty cycle indicates a flip condition.

9. The method of Claim 8, wherein a short duty cycle indicates the flip condition.

10. A transmitter, comprising:

minimum frequency sequence generator receiving parallel data;

a serializer coupled to receive data signals from the minimum frequency sequence generator to output sequential data; and

a clock generator, the clock generator producing a clock signal that indicates whether selected bits of the parallel data have been flipped in the minimum frequency sequence generator.

11. The transmitter of Claim 10, wherein the minimum frequency sequence generator includes

a comparator that sets a flip signal when all of the bits of the parallel data are the same logic level; and

a flip circuit that flips bits of a subset of the parallel data when the flip signal is set.

12. The transmitter of Claim 11, wherein the clock generator alters the duty cycle of the clock signal when the flip signal is set.

13. The transmitter of Claim 12, wherein the duty cycle is set lower when the flip signal is set.

14. A receiver, comprising:

a clock recovery, the clock recovery recovering a clock signal and a flip signal;

a data recovery, the data recovery flipping selected bits in a received bit stream if the flip signal indicates a flipped condition.

15. The receiver of Claim 14, wherein the flipped condition is detected when the duty cycle of the clock signal is lower.

16. A transmitter, comprising:

at least one channel that receives parallel data, the at least one channel including a minimum frequency generator, and a serializer coupled to receive data from the minimum frequency generator;

a sequencer, the sequencer providing an enable signal to the minimum frequency generator of each of the at least one channel; and

a clock generator, the clock generator providing a clock signal,

wherein, the minimum frequency generator of the at least one channel flips a subset of bits of the parallel data and sets a flip flag when all of the bits of the parallel data are the same logic level and the enable signal is set, and

wherein the clock generator encodes whether the flip flag for any of the at least one channels is set.

17. The transmitter of Claim 16, wherein the clock generator shortens the duty cycle of the clock signal the flip flag for any of the at least one channels is set.

18. The transmitter of Claim 16, wherein the sequencer enables each of the at least one channels one at a time in a sequence.

19. The transmitter of Claim 18, wherein the clock generator further encodes a start signal when the sequence of the sequence generator starts.

20. The transmitter of Claim 16, wherein the subset of bits includes half of the parallel bits.

21. An transmitter chip, comprising:

at least one serializer; and

at least one laser diode driver, each of the at least one laser diode driver coupled to one of the at least one serializers,

wherein the at least one serializer and the at least one laser diode driver are formed on a single integrated circuit.

22. The transmitter of Claim 21, further including

at least one minimum frequency generator, each of the at least one minimum frequency generator coupled to one of the at least one serializer, the at least one minimum frequency generator formed on the single integrated circuit.

23. A receiver, comprising:

at least one transimpedance amplifier;

at least one deserializer, each of the at least one deserializer coupled to one of the at least one transimpedance amplifier,

wherein the at least one transimpedance amplifier and the at least one deserializer are formed on a single integrated circuit.

24. The receiver of Claim 23, further including

at least one data recovery circuit, each of the at least one data recovery circuit coupled to one of the ate least one deserializer,

wherein the at least one data recovery circuit is formed on the single integrated circuit.

25. A receiver, comprising:

a clock recovery, the clock recovery recovering a clock signal and a flip signal from a received clock signal;

at least one channel that receives serial data, the at least one channel including a data recovery, the data recovery flipping selected bits in the serial data if the flip signal is set and the at least one channel is selected by an enable signal; and

a sequencer that provides enable signals to each of the at least one channel,

wherein, the data recovery of a selected one of the at least one channel flips bits in the serial data when the selected one of the at least one channel is selected by the enable signal.

26. The receiver of Claim 25, wherein the sequencer enables each of the at least one channels one at a time in a sequence.

27. The receiver of Claim 25, wherein the clock recovery further receives a start signal and wherein the sequencer restarts a sequence in response to the start signal.

28. The receiver of Claim 25, wherein the flip signal is indicated by a shortened duty cycle of the received clock signal.

29. The receiver of Claim 27, wherein the start signal is indicated by a short duty cycle of the received clock signal.